SECONDARY 4
PRELIMINARY EXAMINATION

ELECTRONICS

6063/01

14 August 2024 (Wednesday) **2 hours**

CANDIDATE NAME			
CLASS		INDEX NUMBER	

READ THESE INSTRUCTIONS FIRST
Do not turn over the page until you are told to do so.
Write your name, class, and index number in the spaces provided above.
Write in dark blue or black ink pen.
You may use a soft pencil for any diagrams, graphs or rough working.
Do not use staples, paper clips, highlighters, and glue or correction fluid/tape.

Sections A and B
Answer **all** the questions.
Write your answers in the spaces provided on the question paper.

Approved electronic calculators are allowed for use in this paper.

The number of marks is given in brackets [ ] at the end of each question or part question.

The total mark for this paper is **100**.

FOR EXAMINERS' USE	
Section A	**/ 40**
Section B	**/ 60**
TOTAL	**/ 100**

This document consists of **26** printed pages including the cover page

RESISTOR COLOUR CODE

1st Colour Band 1st Digit		2nd Colour Band 2nd Digit		3rd Colour Band Multiplier		4th Colour Band Tolerance	
Black	0	Black	0	Black	0	Gold	±5%
Brown	1	Brown	1	Brown	1	Red	±2%
Red	2	Red	2	Red	2		
Orange	3	Orange	3	Orange	3		
Yellow	4	Yellow	4	Yellow	4		
Green	5	Green	5	Green	5		
Blue	6	Blue	6	Blue	6		
Violet	7	Violet	7	Violet	7		
Grey	8	Grey	8	Silver	0.01		
White	9	White	9	Gold	0.1		

STANDARD VALUES FOR RESISTORS (E24 SERIES)

1.0 1.1 1.2 1.3 1.5 1.6 1.8 2.0 2.2 2.4 2.7 3.0 3.3
3.6 3.9 4.3 4.7 5.1 5.6 6.2 6.8 7.5 8.2 9.1 and multiples of ten

FORMULAE

Astable and monostable generators using 555 timers

Monostable mode — Period $T = 1.1RC$

Astable mode frequency ($t_1 + t_2$) — Period $T = \dfrac{(R_1 + 2R_2)C}{1.44}$

Bipolar Junction Transistor (BJT)

Current gain — $\beta = \dfrac{\text{Collector current}}{\text{Base current}}$

Voltage gain (for voltage-divider biased CE amplifier, emitter resistor unbypassed)

$$\cong -\frac{R_C}{R_E}$$

[Turn over

Table on Boolean algebra

Single variable theorems	Laws of Complementation	• $\overline{0}=1$ • $\overline{1}=0$ • $\overline{\overline{A}}=A$
	AND Laws	• $A\cdot 0=0$ • $A\cdot 1=A$ • $A\cdot A=A$ • $A\cdot \overline{A}=0$
	OR Laws	• $A+0=A$ • $A+1=1$ • $A+A=A$ • $A+\overline{A}=1$
Multivariable theorems	Commutative Laws	• $A+B=B+A$ • $A\cdot B=B\cdot A$
	Associative Laws	• $A+(B+C)=(A+B)+C=A+B+C$ • $A(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$
	Distributive Laws	• $A\cdot(B+C)=A\cdot B+A\cdot C$ • $(A+B)\cdot(C+D)=A\cdot C+B\cdot C+A\cdot D+B\cdot D$
	Absorptive Laws	• $A+A\cdot B=A$ • $A\cdot(A+B)=A$ • $A+\overline{A}\cdot B=A+B$ • $A\cdot(\overline{A}+B)=A\cdot B$
	DeMorgan's Theorems	• $\overline{(A+B)}=\overline{A}\cdot\overline{B}$ • $\overline{(A\cdot B)}=\overline{A}+\overline{B}$

Section A

Answer **all** questions in this section.

1 Complete Table 1.1

The first row has been completed for you. [5]

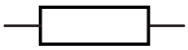
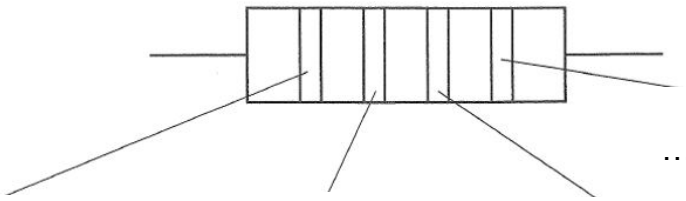
Component name	Component symbol
Fixed resistor	
SPDT switch	
Microphone	
	
	
	

Table 1.1

[Total: 5 marks]

2 The maximum current through a 75 Ω resistor is 80 mA.

(a) Write down the colour code of a 75 Ω resistor with 5% tolerance. [2]



…… ……

…… …… ……

(b) Calculate the maximum power that the resistor will dissipate. [2]

(c) Suggest a suitable power rating for the resistor. Resistors with power ratings of 0.25 W, 0.5 W, 1 W and 2 W are available. [1]

.....

[Total: 5 marks]

3 **(a)** Fig. 3.1 shows the currents entering and leaving three circuit nodes.

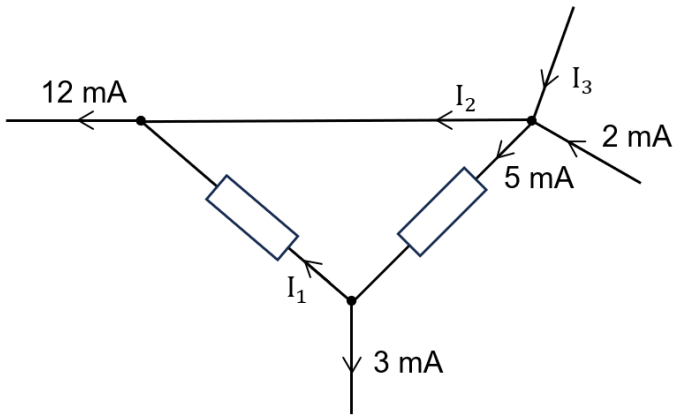


Fig. 3.1

Complete Table 3.1. [3]

Current	Value
I_1	
I_2	
I_3	

Table 3.1

(b) Fig. 3.2 shows a circuit with two voltage sources.

The direction of current through each resistor is indicated with an arrow in Fig. 3.2.

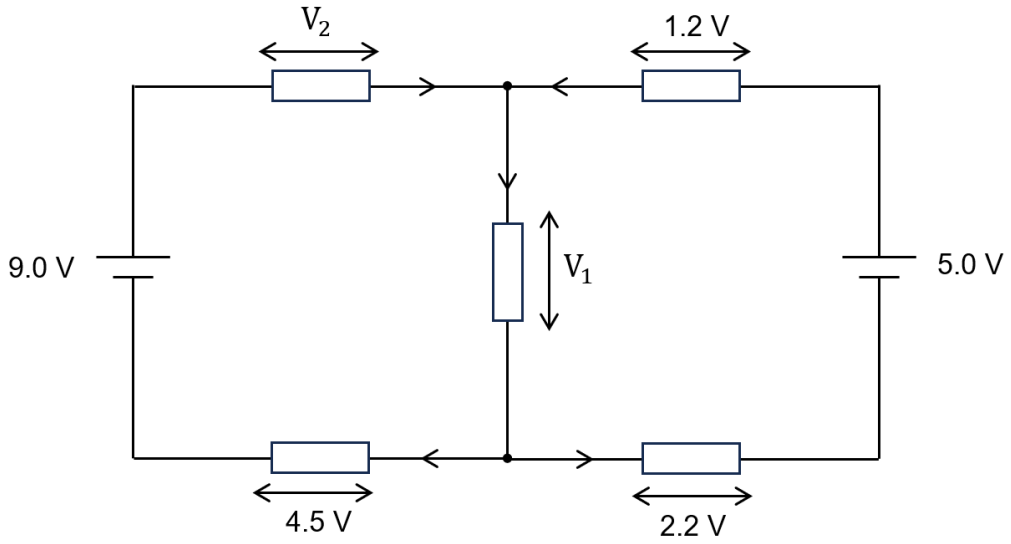


Fig. 3.2

Complete Table 3.2. [2]

Voltage	Value
V_1	
V_2	

Table 3.2

[Total: 5 marks]

4 A rectangular signal has the following characteristics:

- Frequency = 200 Hz
- Duty cycle = 40%
- Low level voltage = 0 V
- High level voltage = 5 V

(a) On Fig. 4.1, draw the waveform of the rectangular signal when connected to a digital oscilloscope. The oscilloscope uses the following settings:

- horizontal scale: 1 ms / div
- vertical scale: 2 V / div [3]

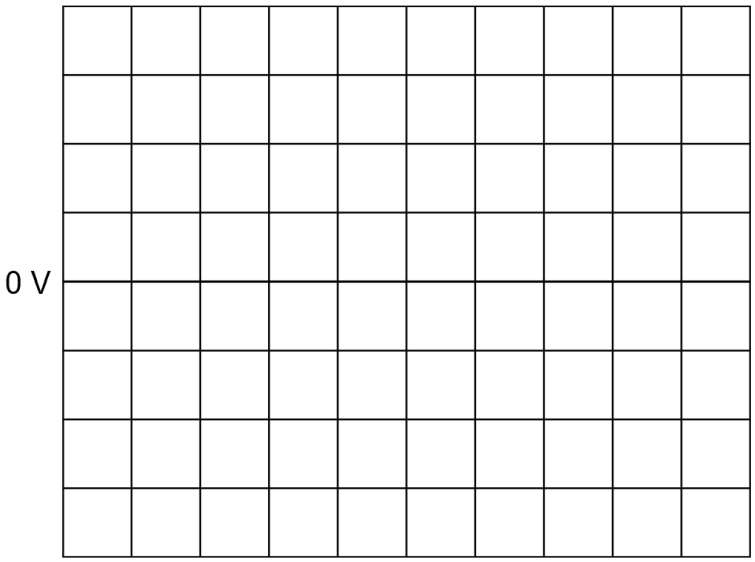


Fig. 4.1

(b) A rectangular signal is periodic. Explain what is meant by a *periodic signal*. [1]

.....

.....

[Total: 4 marks]

5 Fig. 5.1 shows two capacitors, X and Y.

Capacitor X Capacitor Y

Fig. 5.1

(a) Write down the capacitance of capacitor X. [1]

.....

(b) Capacitor Y has a capacitance of 2200 μF.

Besides their capacitance values, state another difference between capacitors X and Y. [1]

.....

.....

[Total: 2 marks]

6 Fig. 6.1 shows an incomplete circuit diagram of a full-wave rectifier.

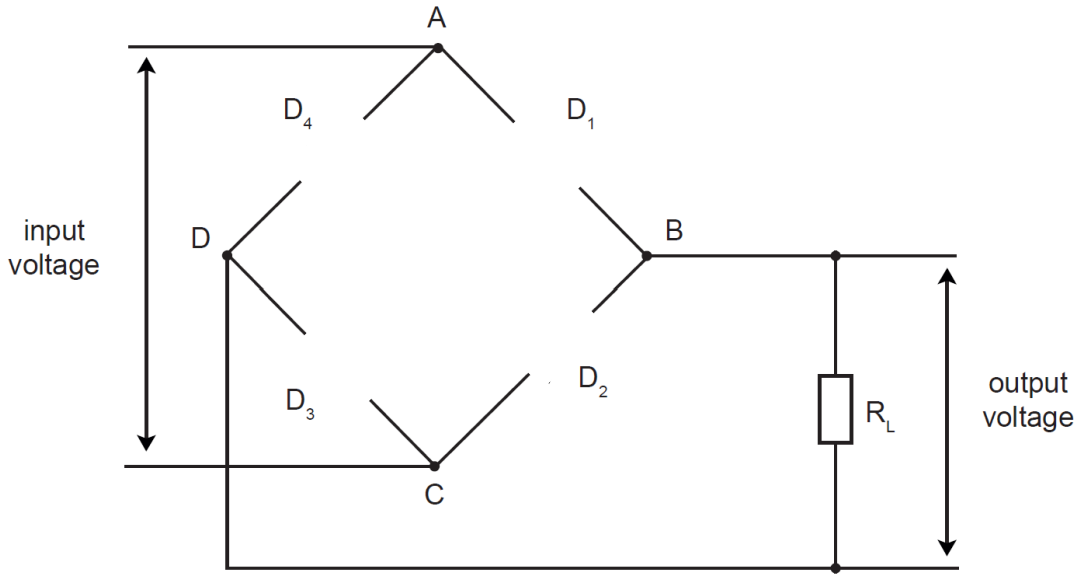


Fig. 6.1

(a) Complete Fig. 6.1 by drawing four diodes. [2]

(b) State the property of diodes that a full-wave rectifier makes use of. [1]

.....

(c) Fig. 6.2 shows how the input voltage varies with time. Complete Fig. 6.3 to show how the output voltage varies with time. [2]

Use the ideal diode model.

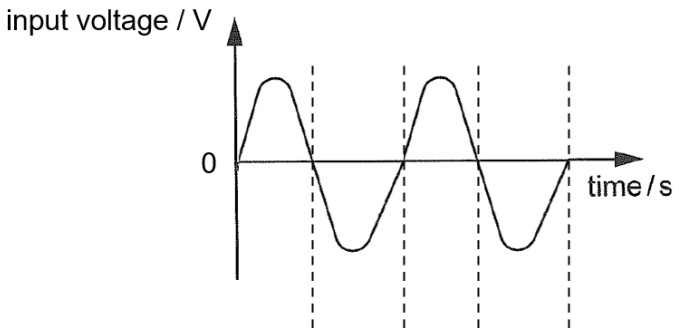


Fig. 6.2

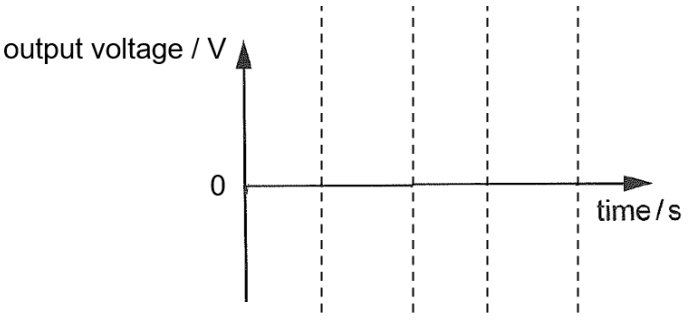


Fig. 6.3

[Total: 5 marks]

7 Fig. 7.1 shows an incomplete circuit with a logic switch consisting of a pushbutton switch, S_1 and a resistor, R_1.

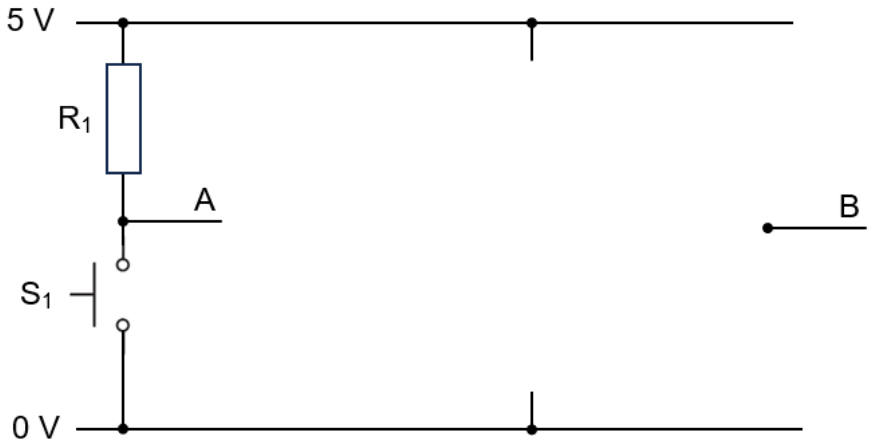


Fig. 7.1

(a) Complete Table 7.1 to show the logic state of the signal at A. [1]

Switch S_1	Logic state of signal at A
Open	
Close	

Table 7.1

(b) Describe and explain the purpose of resistor R_1. [2]

…….....……

.....……

(c) Complete Fig. 7.1 to show how a NPN bipolar junction transistor can be wired to produce at signal at B that is opposite logic state as the signal at A.

Show any additional components needed for the solution. [3]

[Total: 6 marks]

8 NAND gates and NOR gates are universal gates.

(a) Explain what is meant by *universal gate*. [1]

……...….

……....

(b) By drawing circuit diagrams, show how an AND gate can be implemented using only

(i) NAND gates, [1]

(ii) NOR gates. [2]

[Total: 4 marks]

9 **(a)** Add the following two binary numbers together and write the answer in binary-coded decimal. [1]

0101 + 1001 = ...

(b) Convert the answer from **(a)** into binary. [1]

(c) Write down one advantage and one disadvantage of using binary-coded decimal over binary. [2]

Advantage .....

.....

Disadvantage .....

.....

[Total: 4 marks]

Section B
Answer **all** questions in this section.

10 Fig. 10.1 shows the pin connection diagram of a 555 timer IC.

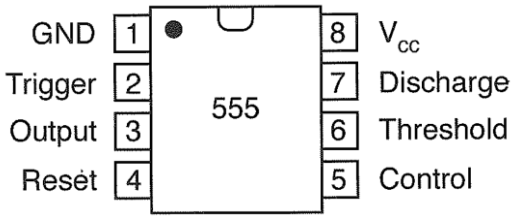


Fig. 10.1

Fig. 10.2 shows a 555 timer IC connected as an astable multivibrator to produce a blinking light.

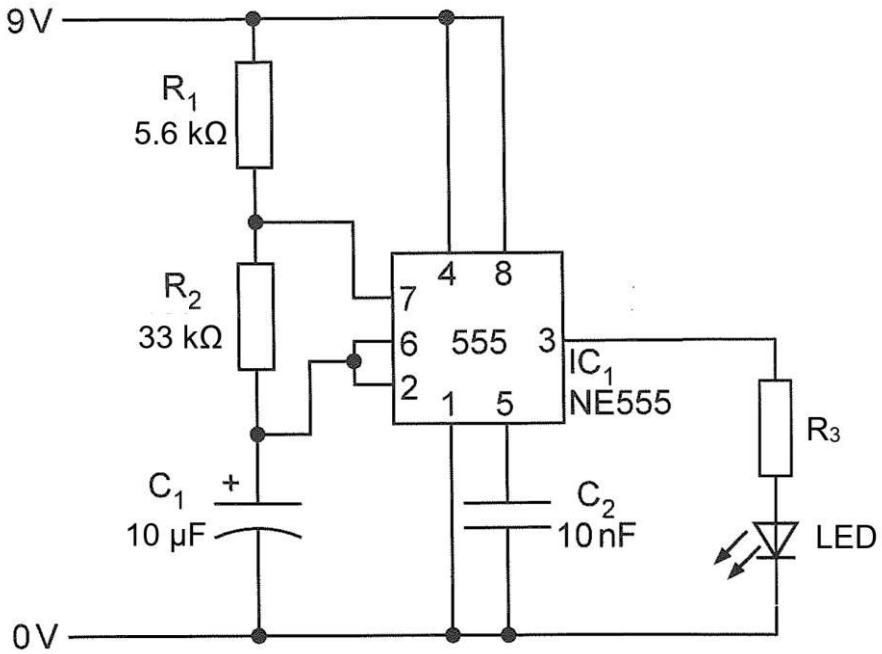


Fig. 10.2

(a) Complete Table 10.1 by stating the function of pins 2 and 6. [4]

Pin Number	Name of Pin	Function
2	Trigger	
6	Threshold	

Table 10.1

[Turn over

(b) Calculate the period of the output signal at pin 3. [2]

(c) Explain, in terms of R_1 and R_2, why the duty cycle of the output signal is always more than 50%. [1]

.....

.....

.....

(d) Calculate the amount of charge stored in C_1 when the pin 2 is 4.0 V. [2]

(e) A student connected another 10 μF capacitor in parallel with C_1.

State and explain the effect on the period of the output signal. [3]

.....

.....

.....

.....

(f) The output voltage of the 555 timer IC in Fig. 10.2 is 8.1 V for HIGH state. The LED has a forward voltage of 2.0 V and an operation current of 20 mA.

Determine a suitable E24 resistor value for R_3. [3]

[Total: 15 marks]

11 The organiser of Pokémon Go game needs to generate a list of participants who qualify for the master trainer challenge.

To qualify, a participant must achieve at least two of the following criteria:

- defend a Gym for at least ten times
- achieve at least Level 30
- collect at least 3 legendary Pokémons

You are tasked to design the combinational logic circuit shown in Fig. 11.1 to generate the list.

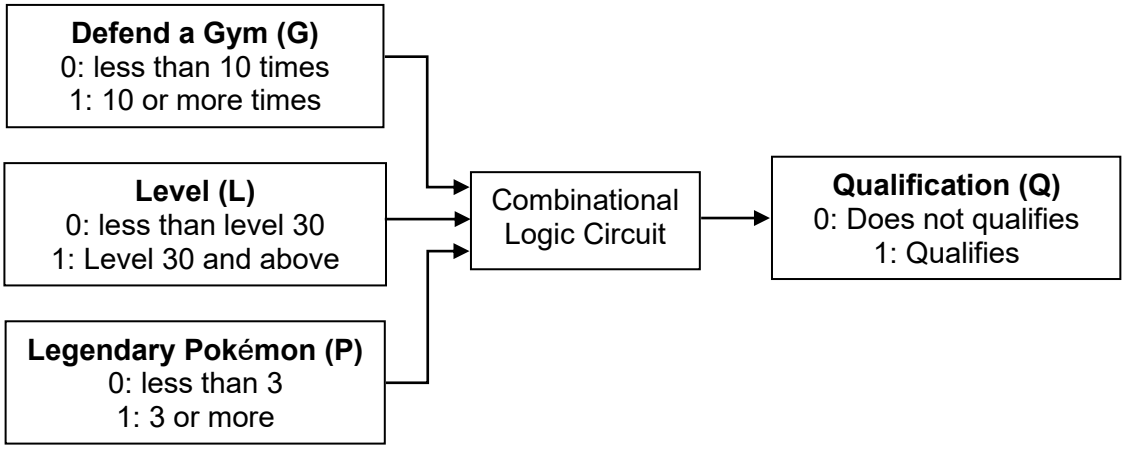


Fig. 11.1

(a) Complete the truth table in Table 11.1 based on the criteria. [3]

G	L	P	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 11.1

(b) Write the Boolean expression of the combination logic based on Table 11.1. [1]

Q = ……

(c) Simplify the Boolean expression from **(b)** using the Karnaugh map shown in Fig. 11.2. The loops should be clearly shown. [3]

G \ LP	00	01	11	10
0				
1				

Fig. 11.2

(d) Write the simplified Boolean expression based on the Karnaugh map from **(c)**. [1]

Q = ……..…….....

(e) In the space below, draw the logic circuit that represents the Boolean expression from **(d)**. [3]

(f) Fig. 11.3 shows the simplified diagram of a 74LS08 IC.

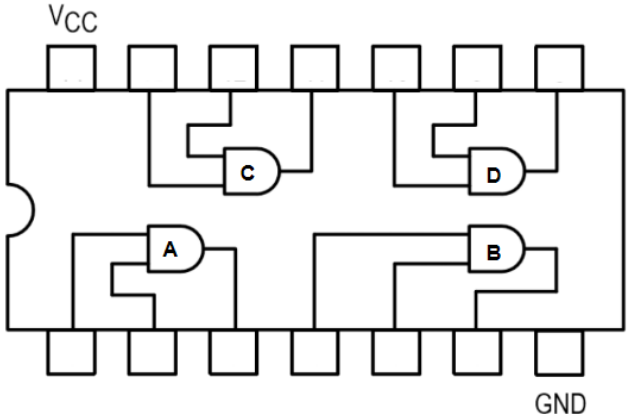


Fig. 11.3

(i) Complete Table 11.2 to state the functions of Pins 6 and 14 of the 74LS08 IC. [2]

Pin number	Function
14	
6	

Table 11.2

(ii) State what IC stands for. [1]

……..……..……...

(iii) The datasheet of 74LS08 indicates that the minimum value of V_{IH} is 2.0 V. Explain what V_{IH} means. [1]

……..……..……...

……..……..……..

[Total: 15 marks]

12 Fig. 12.1 shows a temperature-controlled circuit.

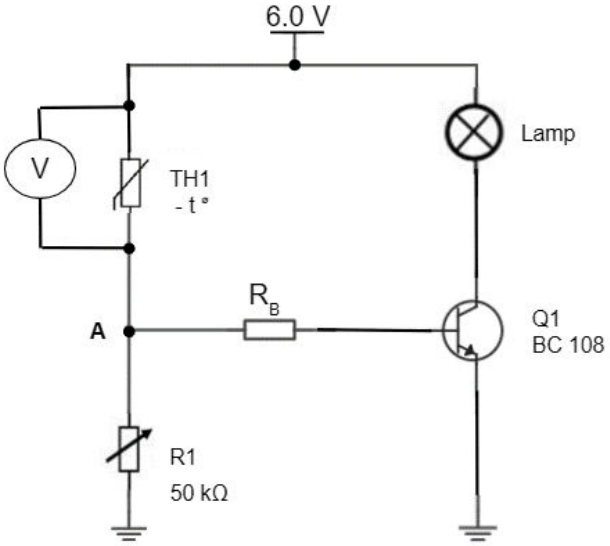


Fig. 12.1

The lamp has a current rating of 350 mA.

Table 12.1 shows several specifications of transistor Q1, extracted from its datasheet.

Transistor Model	BC108
β_{dc}	300
$V_{CE(sat)}$	0.20 V
V_{BE}	0.70 V

Table 12.1

(a) State the purpose of variable resistor R1. [1]

……

(b) When the temperature is 20 °C, the resistance of TH1 is 30 kΩ.

The variable resistor R1 is set to 65% of 50 kΩ.

(i) Calculate the voltage at point A. [2]

(ii) Determine the resistance of R_B when I_B is 100 μA. [2]

(c) State and explain what will happen to the voltmeter reading if the temperature increases. [2]

……

……

……

(d) The current through the base of the BC108 transistor, I_B, is 100 μA.

Explain why the BC108 transistor is unable to cause the lamp to operate at its rated current of 350 mA. [2]

.....

.....

(e) Fig. 12.2 shows an additional transistor, Q2, added to the circuit shown in Fig. 12.1.

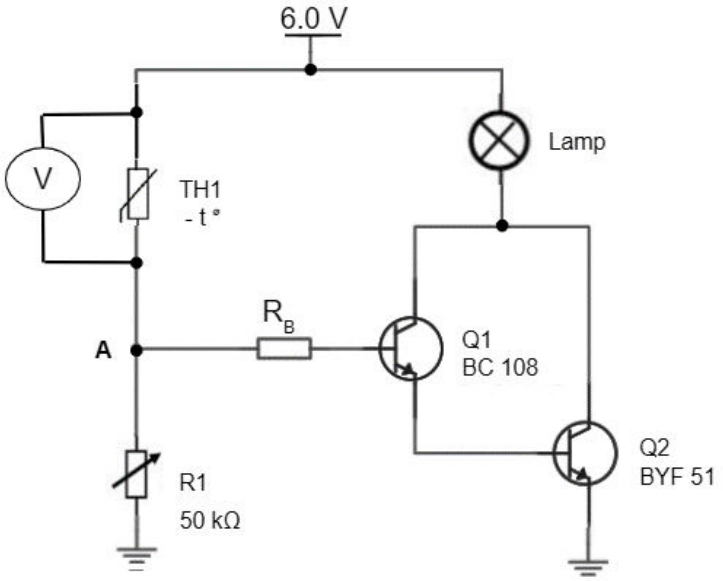


Fig. 12.2

Table 12.2 shows several specifications of the two transistors, extracted from their datasheets.

Transistor Model	BC108	BYF51
β_{dc}	300	40
$V_{CE(sat)}$	0.20 V	0.20 V
V_{BE}	0.70 V	0.70 V

Table 12.2

$V_{CE(sat)}$ = 0.90 V (transistor pair)

(i) Name the configuration of transistors Q1 and Q2. [1]

……..……..……..……

(ii) Calculate the saturation current, $I_{c(sat)}$, when the resistance of the lamp is 17 Ω. [2]

(iii) Using answer in **(ii)**, calculate the base current $I_{B(sat).}$ [2]

(iv) Suggest one possible modification to the circuit so that the lamp operates in its rated current of 350 mA. [1]

……..……..……..……

……..……..……..……

[Total: 15 marks]

13 Fig. 13.1 shows a production line and block diagram where products are counted as they move along a conveyor belt.

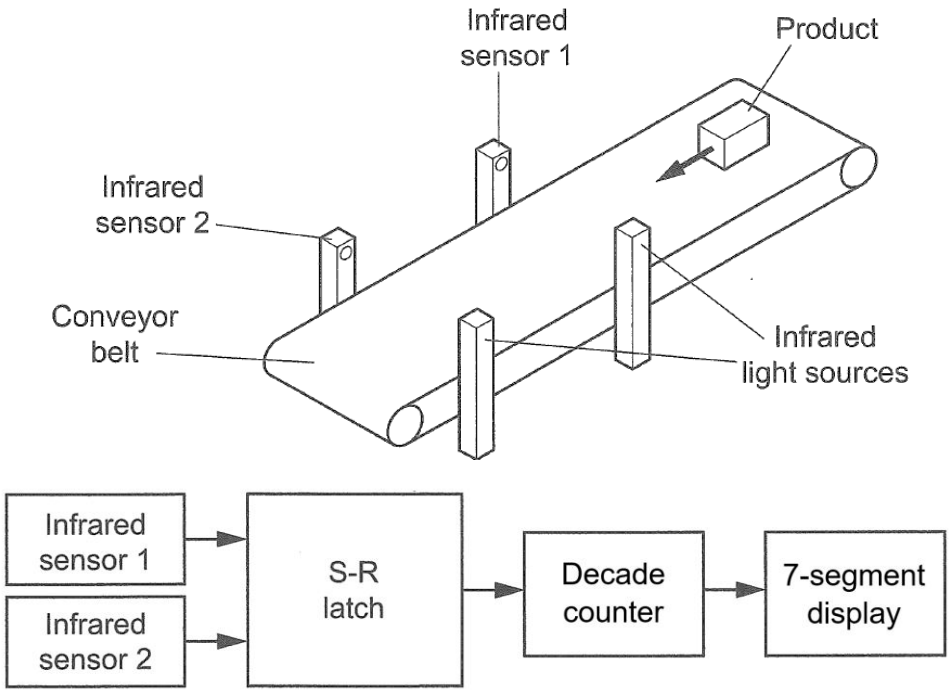


Fig. 13.1

There are two identical infrared (IR) sensor subsystems. Each sensor subsystem comprises an IR light source which emits a beam of IR towards an IR sensor.

Products must move along the conveyor belt and pass through both beams to register with a counter.

Fig. 13.2 shows the incomplete circuit diagram of one of the infrared sensor subsystems and the S-R latch.

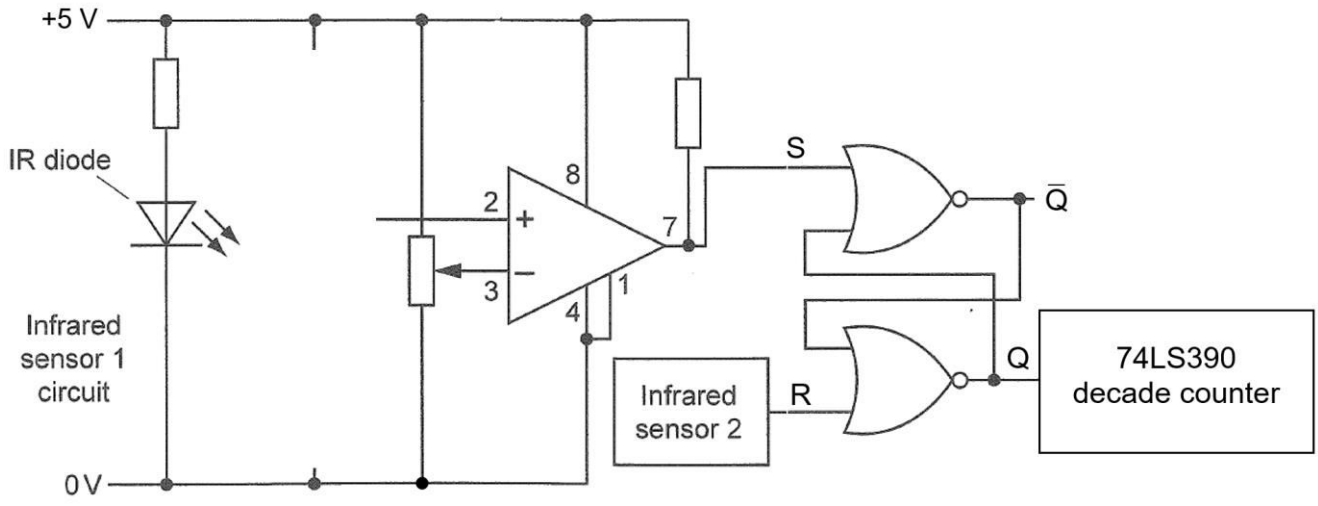


Fig. 13.2

(a) The infrared sensor uses a photodiode. Explain how a photodiode works. [2]

.....

.....

.....

(b) Complete Fig. 13.2 by adding a resistor and a photodiode so that the voltage at the non-inverting input of the comparator is

- close to 5 V when the IR beam is blocked,
- close to 0 V when the IR beam is not blocked. [2]

(c) The inverting input of the comparator is connected to a potentiometer. Explain the advantage of using a potentiometer instead of two fixed resistors. [1]

.....

.....

(d) Table 13.1 shows the truth table of the system as the product moves along the conveyor belt. Complete Table 13.1 with the logic state of the signals. [4]

Position of product on belt	S	R	Q	$\overline{Q}$
before infrared sensor 1	0	0	0	1
at infrared sensor 1				
between infrared sensor 1 and 2				
at infrared sensor 2				
after infrared sensor 2				

Table 13.1

(e) Using your answers in Table 13.1, suggest why output Q of the S-R latch is used as the CLK signal for the decade counter instead of output $\overline{Q}$. [1]

.....

.....

(f) Fig, 13.3 shows the pin connection diagram of a 74LS390 decade counter IC.

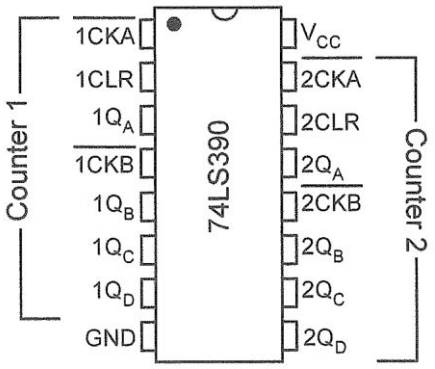


Fig. 13.3

Using the information from Fig. 13.3 complete Fig. 13.4 so that both the decade counters in the 74LS390 work together to count to 99. [2]

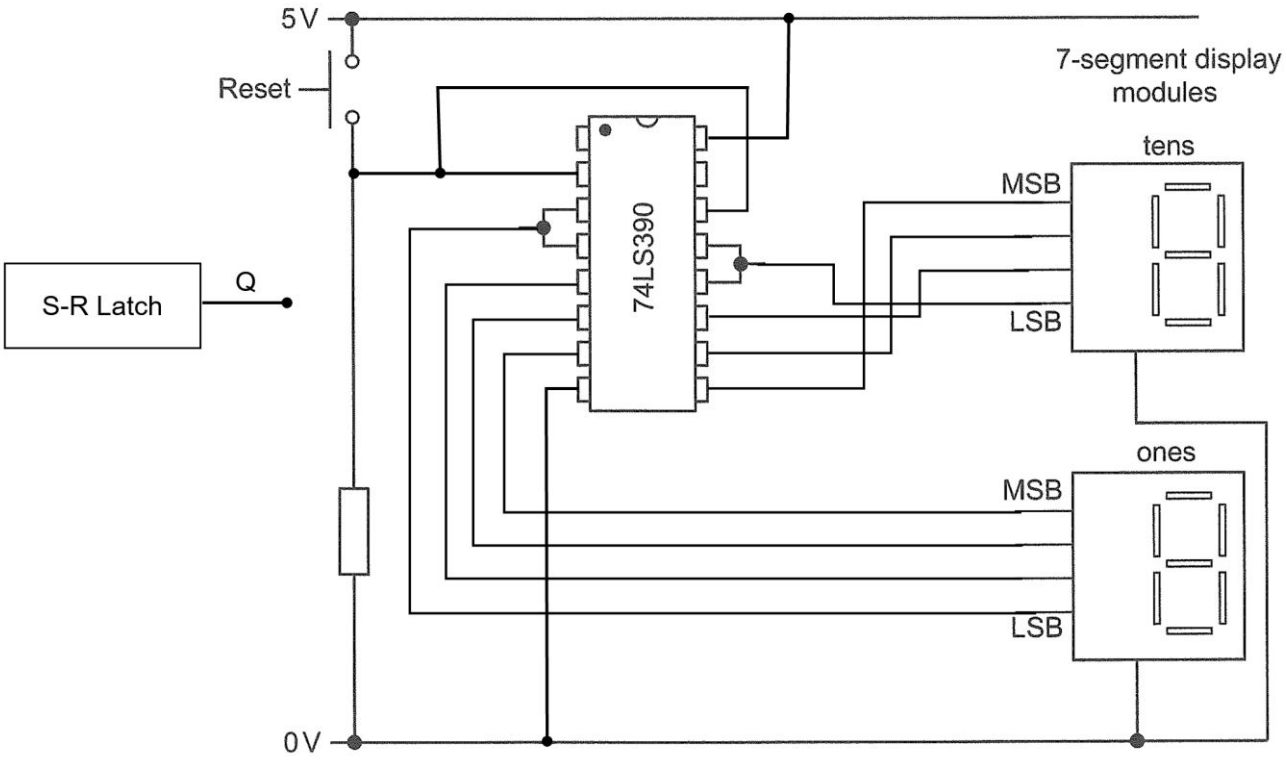


Fig. 13.4

(g) **(i)** Complete the Table 13.2 to show the logic state of outputs Q_D to Q_A when the count value is 99. [1]

Count Value (decimal)	Counter 2				Counter 1			
	$2Q_D$	**$2Q_C$**	**$2Q_B$**	**$2Q_A$**	**$1Q_D$**	**$1Q_C$**	**$1Q_B$**	**$1Q_A$**
99								

Table 13.2

(ii) A new signal, S, is required. Signal S should go HIGH only when the count value reaches 99.

Using only logic gates from the list below, complete Fig. 13.5 to show how signal S can be produced.

- NOT gates
- 2-input AND gates
- 2-input OR gates
- 2-input NAND gates
- 2-input NOR gates [2]

$2Q_D$ ——

$2Q_C$ ——

$2Q_B$ ——

$2Q_A$ ——

—— S

$1Q_D$ ——

$1Q_C$ ——

$1Q_B$ ——

$1Q_A$ ——

Fig. 13.5

[Total: 15 marks]

END OF PAPER